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EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,514	GILBERT, BARRIE	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *28-31* is/are allowed.

6)☒ Claim(s) *12,13,15,17,19,21,22 and 24-26* is/are rejected.

7)☒ Claim(s) *14,16,18,20,23 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's appeal brief filed on 11/21/05 is acknowledged. In view of the current reconsideration, new grounds of rejections to some of the claims are needed as set forth below. This action is NON-FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 12-13, 15, 19, 21-22 and 24-25 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 5,909,136, issued to Kimura.

As per claim 12, Kimura discloses a squaring cell (Fig. 5) comprising:

a first sub-exponential current generator (the combination of Q1, Q2, Q5-Q9 and current source 31) for generating a first current (the current at the collector of Q9, the limitation "sub-exponential" is met because formula 17 shown in column 8 is merely the approximation of the first current, see column 8, lines 3-6, i.e., Kimura assumes current gain factor is 1 (which is not) when deriving formula 17) responsive to an input signal Vi (at nodes 11 and 12); and

a second sub-exponential current generator (the combination of Q3-Q4, Q10-Q14 and current source 32) for generating a second current (at the collector of Q14) responsive to the input signal Vi;

wherein the first and second sub-exponential current generators are coupled together (at node 13) to combine the first and second currents.

As per claim 13, Kimura further discloses each of the sub-exponential current generator includes:

a constant current stack (transistors Q1 and current source 31, i.e., Q1 and current source 31 are stacked and current source 31 has constant current I0) coupled to a first input terminal 11; and

a variable current stack (Q2 and Q5 are stacked and the current through Q2 is not constant) coupled to a second input terminal 12 and the constant current stack (Q1 and Q2 are connected).

As per claim 15, this claim is merely a method to operate the squaring cell having elements and connections discussed in claim 12 above. Since Kimura teaches the circuit, he inherently teaches the recited method.

As per claim 19, the same rejection as discussed in claim 12, and further, since Kimura discloses current source I0 is programmable parameter (column 8, line 58), he inherently discloses the recited limitation which is altering the first and second currents. The recited limitation is also met since the input voltage VI is not a constant voltage. Also, since the first and second currents are altered, the exponential functions are modified.

As per claim 21, Kimura discloses a multiplier (Fig. 1) comprising:

a first exponential current generator (Fig. 1, box 1, Fig 5 is the detail, transistors Q1, Q2, Q5-Q9, current source 31) for generating a first current (at the collector of Q9) responsive to a first input signal Vx and second input signal -Vy;

a second exponential current generator (Fig, 1, box 1, Fig. 5 is the detail, transistors Q3-Q4, Q10-Q14, current source 32) for generating a second current (at the collector of Q14) responsive to a third input signal Vx and a fourth input signal Vy (Note that the first and third input signals are the same);

a third exponential current generator (Fig. 1, box 2, Fig. 5 is the detail, transistors Q1, Q2, Q5-Q9, current source 31) for generating a third current (at the collector of Q9) responsive to the first input signal Vx and the fourth input signal Vy;

a fourth exponential current generator (Fig. 1, box 2, Fig. 5 is the detail, transistors Q3-Q4, Q10-Q14, current source 32) for generating a fourth current (at the collector of Q14) responsive to the third input signal Vx and the second input signal -Vy;

wherein the first and second sub-exponential current generators are coupled together (at node 13) to combine the first and second currents.

wherein the third and fourth exponential current generators are coupled together (at node 13) to combine the third and fourth currents.

As per claim 22, this claim is rejected for the reason discussed in claim 13.

As per claim 24, this claim is merely a method to operate a multiplier having the structure noted in claim 21. Since Kimura teaches the circuit, he inherently teaches the recited method.

As per claim 25, the steps of combining are performed at nodes 13 shown in Fig. 1.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,909,136, issued to Kimura. in view of US Patent No. 6,173,346, issued to Wallach et al.

As per claim 17, Kimura discloses steps for squaring a signal as discussed in claim 12, and further, Kimura explicitly discloses the current source I0 is a programmable parameter (column 8, line 58). In other words, he discloses the current source I0 can be scaled in response to a control signal so that the first and second currents are scaled.

Kimura does not explicitly disclose the step of scaling is performed while generating and combining the first and second currents. In other words, Kimura does not explicitly disclose the step of programming the current source I0 is performed while the circuit is operating.

Wallach discloses in the abstract that adding or replacing a functionality of a circuit using software architecture, i.e., programming, without power down the system, i.e., hot swap, is a desirable feature. Wallach's reference is clearly in the field of applicant's endeavor, i.e., electronic circuits and pertinent to the particular problem which is to modify a parameter of the circuit while the circuit is operating.

It would have been obvious to one skilled in the art at the time of the invention was made to perform the step of scaling in the Kimura's circuit while the circuit is operating as taught by

Wallach. The motivation and/or suggestion would be to save the time needed to power down the system.

As per claim 26, rejected for the same reason and motivation discussed in claim 17.

Response to Arguments

4. Applicant's arguments filed 2/22/05 have been fully considered but they are not persuasive.

Regarding the argument that Kimura does not disclose a sub-exponential current generator as required by the claim. Kimura does not disclose any structure for deliberately changing the exponential function of an exponential current generator.

As discussed in the preceding rejection, Kimura teaches that transistors used in the exponential current generator circuits do not have exactly the same geometry, the exponential current generator circuits do not generate ideal exponential functions. In other words, the Kimura's exponential current generator circuits are sub- exponential current generator circuits. Claim 12 requires the exponential current generators generate sub-exponential functions, the Kimura's exponential current generators generate sub-exponential functions as discussed above, the recited limitation is met. The act of "deliberately" is irrelevant because the claim only requires the exponential current generator circuits generate sub-exponential functions, and the Kimura's exponential current generators clearly generate sub-exponential functions.

Other arguments are moot in view of new grounds of rejections.

Allowable Subject Matter

5. Claims 14, 16, 18, 20, 23 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The claims are allowable for the reasons noted in the previous Office action.

6. Claims 28-31 are allowed. The claims are allowed for the reasons noted in the previous Office action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 571-272-1748. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

2/4/06

Minh Nguyen
Primary Examiner
Art Unit 2816